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The Ambient Temperature Effect on Current-Voltage Characteristics of Surface-Passivated GaN-Based Field-Effect Transistors

W.L. Liu, V.O. Turin, A.A. Balandin
Nano-Device Laboratory, Department of Electrical Engineering, University of California - Riverside

Y.L. Chen, K.L. Wang
Device Research Laboratory,Electrical Engineering Department,University of California - Los Angeles.

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Abstract

We have studied experimentally the effect of ambient temperature on performance of the surface-passivated $Al_{0.2}Ga_{0.8}N$/GaN heterostructure field-effect transistors in the temperature range from 25°C to 250°C. The measured data have been compared with physics-based modeling of the GaN transistor characteristics under different ambient temperatures. The experimental data, showing about 33% degradation in the saturation current with a temperature increase from 25°C to 250°C, agrees well with the results of simulations performed using ISE DESSIS software. Obtained results and analytical extrapolations can be used for predicting device performance in changing environments, as well as for optimization of the device structure.

1. Introduction

GaN-based heterostructure field-effect transistors (HFETs) are attracting attention as promising candidates for high-frequency high-power applications. AlGaN/GaN HFETs have demonstrated the ability to operate at frequencies above 10 GHz while providing power levels exceeding 11 W/mm [1] [2]. These devices are capable of working with low flicker noise levels (Hooge parameter $\alpha_H \approx 10^{-4}$~10^{-5}) comparable to those in Si and GaAs devices [3] [4]. For applications in remotely controlled vehicles and satellites, the stability of device operation under changing temperature is of critical importance. An increase in ambient temperature coupled with strong self-heating effects in high-power GaN transistors may result in significant performance degradation. The thermal structure resistance also increases at high temperature due to the decrease of the thermal conductivity K, which falls off as $\sim 1/T^{0.5}$ in GaN films [5] [6] [7]. In this paper we report results of experimental investigation and computer simulation of the effect of ambient temperature on performance of the SiO_2-passivated $Al_{0.2}Ga_{0.8}N$/GaN HFETS.

2. Experiment

The $Al_{0.2}Ga_{0.8}N$/GaN heterostructure was grown on a semi-insulating SiC substrate by metal organic chemical vapor deposition technology. The structure consists of 1.2 μm undoped GaN, 50 nm undoped GaN channel layer, 3 nm undoped $Al_{0.2}Ga_{0.8}N$ spacer and 15 nm Si doped (N_D=6×10^{18}cm^{-3}) $Al_{0.2}Ga_{0.8}N$ barrier layers. HFETs with gate dimension of 1 μm × 20 μm, and the gate-source and gate-drain distances of 1 μm have been fabricated on this heterostructure. Mesa isolation is achieved by ion implantation of As^+ at 75 keV and dose1.27×10^{11} cm^2, As^+ at 375 keV and dose 4.32×10^{11} cm^2, and He^+ at 75 keV and dose 5.43×10^{11} cm^2. The source - drain ohmic contacts are formed by Ti/Al/Ni/Au (200Å /800Å /400Å /1500Å) multilayer. The gate Schottky contact is formed by Pd/Au (200Å/6500Å) layer. Before metal

deposition, O_2 descum and BOE etching were conducted on the Schottky area to remove residues and the thin oxide layer. After the above processes are finished, a 270 nm SiO_2 layer was deposited by plasma enhanced chemical vapor deposition to provide surface passivation. The transistor current-voltage (IV) characteristics were measured using a HP4142B-based parameter analyzer connected to the Signatone probe station with a hot chuck.

3. Physics-Based Modeling

The physics-based ISE DESSIS software has been used for simulation of the temperature dependent IV characteristics of the GaN-based field-effect transistors. The physical parameters defining the electron and thermal transport properties of GaN material have been taken from recently published works [5] [8] [9] [10] [11] [12] [13]. For simplicity the 2D simulations were carried out for a metal-semiconductor field-effect transistor with the following parameters: the doping concentration in the active layer is 3×10^{17} cm^{-3}; the thickness of the active layer is 200 nm. The source - drain separation L_{SD} = 3 μm and the gate length L_G = 1 μm are chosen to be the same as in the actual transistors under test. The active n-GaN channel is on the top of 3 μm thick semi-insulating GaN buffer layer. The device structure was assumed to be on a 300 μm thick SiC substrate. The simulation domain size along the substrate was 1500 μm. We have adopted the low-field mobility model from Ref. [8]. The high-field mobility has been calculated using the Canali model [9]:

$$\mu_{high} = \mu_{low} \Big/ \left(1 + \left(\mu_{low} E / v_{sat}\right)^{\beta_0}\right)^{1/\beta_0} \tag{1}$$

The electron saturation velocity v_{sat} = 1.91×10^7 cm/s at 300 K was extracted from the Monte-Carlo simulation results [10]. The coefficient for the linear dependence of the saturation velocity on temperature was assumed to be -6.33×10^3cm/s K. This parameter was obtained by fitting the data from the Monte Carlo simulations reported in [11].

The basic equations used in the drift-diffusion model (DDM) simulation include Poisson, electron continuity, hole continuity and thermal conductivity equations

$$\begin{cases} \nabla \varepsilon \cdot \nabla \varphi = -e\left(p - n + N_D - N_A\right) \\ \dfrac{\partial n}{\partial t} = \dfrac{1}{e}\nabla \cdot \vec{j}_n + G_n - R_n \\ \dfrac{\partial p}{\partial t} = -\dfrac{1}{e}\nabla \cdot \vec{j}_p + G_p - R_p \\ c\dfrac{\partial T}{\partial t} - \nabla \cdot k(T)\nabla T = -\nabla \cdot \left(\phi_n \vec{j}_n + \phi_p \vec{j}_p\right) \end{cases} \tag{2}$$

The current densities for electrons and holes are given as

$$\begin{aligned} \vec{j}_n &= -nq\mu_n \nabla \phi_n \\ \vec{j}_p &= -pq\mu_p \nabla \phi_p \end{aligned} \tag{3}$$

In the above equations we adopted the standard notations in their conventional meaning. For the electrical boundaries without contacts, the reflective boundary conditions are applied. For the Schottky contact, the boundary conditions are defined as

$$\begin{aligned}
\varphi &= V_g - \Phi_B + \frac{kT}{q}\ln\left(\frac{N_C(T)}{n_i}\right) \\
\vec{J}_n \cdot \vec{N} &= q\upsilon_n\left(n - n_0^B\right) \\
\vec{J}_p \cdot \vec{N} &= q\upsilon_p\left(p - p_0^B\right) \\
n_0^B &= N_C(T)\exp\left(\frac{-q\Phi_B}{kT}\right) \\
p_0^B &= N_V(T)\exp\left(\frac{-E_G + q\Phi_B}{kT}\right)
\end{aligned} \tag{4}$$

The Schottky barrier height Φ_B is the difference between the metal work function and the electron affinity of the semiconductor. Here we assume it is equal to a typical value of 1 eV. n_0^B and p_0^B are the equilibrium electrons and holes densities at contact surface, respectively. The values for the thermionic emission velocities v_n and v_p are 2.573×10^6 cm/s and 1.93×10^6 cm/s respectively. To close the thermal equation, the isothermal boundary condition is assumed for the bottom of the substrate, where the temperature is equal to that of ambient, and the adiabatic boundary is assumed for the top and lateral surface. Room temperature thermal conductivities for SiC and GaN are taken from Ref. [12]. The $T^{-0.5}$ temperature dependence for thermal conductivity of GaN [5] [6] [7] and T^{-1} for SiC [12] has been adopted in the simulations. The details of the simulation approach based on the solution of the carriers drift-diffusion and thermal diffusion equations were described elsewhere. [13] A posterior comparison with experiments attests that the simplified model for the transistor is capable of capturing the main features of ambient heating effects in AlGaN/GaN HFETs.

4. Results

In Figure 1 we present typical measured DC IV characteristics of SiO_2-passivated $Al_{0.2}Ga_{0.8}N$/GaN HFET with the gate bias changing from 1V to - 4V. The data is shown for two ambient temperatures T=25°C and T=250 °C. One can see the reduction of the current with increased ambient at each value of the gate bias. The saturation current reduction is caused by degradation of the electron mobility due to increased electron - phonon scattering. The decrease of the saturation current at zero gate bias when temperature increases to 250 °C is about 33%. Figure 2 shows the saturation current as a function of temperature at V_g=0V. The saturation current is normalized to its room-temperature value. In the examined range of temperatures the decrease is linear and can be approximated as $I_{sat}/I_{sat}(T$=25^{o}degree;C)=1.03-0.0013·T, where T is measured in ^{o}degree;C.

The experimental dependence of the transconductance on ambient temperature is presented in Figure 3. For tested HFETs the maximum transconductance is achieved at about –1V ~ –2V, while the threshold voltage is about -4V. One observes that as the ambient temperature increases the transconductance peak decreases and shifts toward the lower bias voltage. Compared with the room-temperature value, the maximum transconductance at 250^{o}degree;C decreases by ~ 33 percent. The small shift in the peak position can be attributed to some increase in the gate leakage current. The gate metal Pd/Au contact used in the tested devices showed very good thermal stability over the measured temperature range.

In order to estimate the reliability of the system, it is important to be able to predict changes in transistor IV characteristics with varying ambient temperature. The results of the computer simulation of IV characteristics of GaN-based transistor for T=25^{o}degree;C and T=250^{o}degree;C are shown in Figure 4 with the solid and dashed curves, respectively. Comparing with Figure 1, one can see that the degradation trend in the saturation current is captured by the simulation results very well. The change in the current value with temperature increase to 250^{o}degree;C is about 36%, which is very close to experimentally observed decrease.

4.1. Conclusions

We investigated the effect of ambient temperature on the performance of the SiO_2-passivated $Al_{0.2}Ga_{0.8}N$/GaN HFETs in

the temperature range from 25°C to 250°C. The experimental data indicates ~33% degradation in the saturation current and transconductance with temperature increase to 250^{o}degree;C. The results of computer simulations performed using the ISE DESSIS software with GaN parameters and material-specific models for the carrier and heat transport are in good agreement with the experimental data. Obtained experimental dependencies and modeling approach can be used for predicting GaN-based device performance under changing ambient temperature.

Acknowledgments

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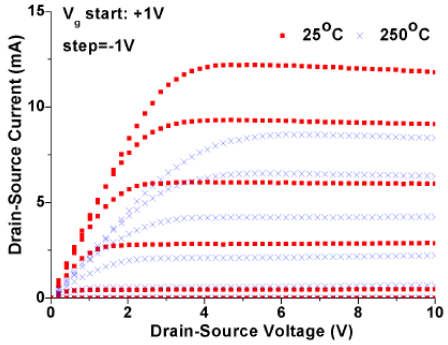
Figure 1. Current-voltage characteristics of the surface-passivated AlGaN/GaN HFET at two different ambient temperatures 25°C (squares) and 250°C (crosses), respectively.



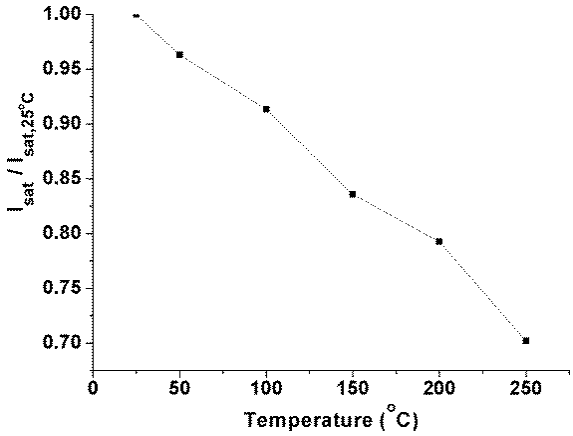


Figure 2. Measured saturation current at V_g=0V as a function of the ambient temperature. The data are normalized to the current value at room temperature.

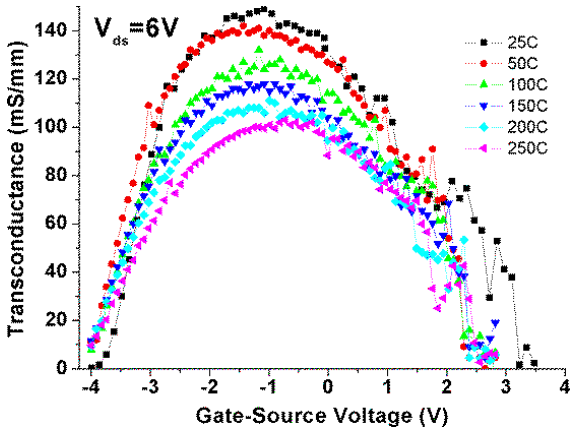
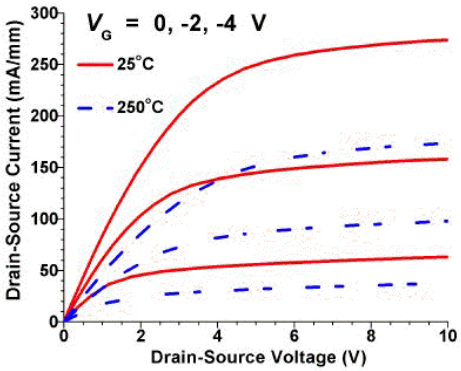


Figure 3. Measured transconductance as a function of the gate bias at different ambient temperature.

Figure 4. Simulated current-voltage characteristics for GaN-based field-effect transistor at two different temperatures 25°C (solid curves) and 250°C (dashed curves), respectively.



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